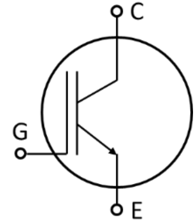
IGBT Chip

Features:

- 1050V Trench & Field stop technology
- Low switching losses
- Positive temperature coefficient
- Easy paralleling

Applications:

- 3-level-applications
- Solar applications



Mechanical parameters

Die size	9.58×9.58	mm^2
Emitter pad size	See chip drawing	
Gate pad size	1.40×0.80	
Area total	91.78	
Thickness	95	µm
Wafer size	300	mm
Max. possible chips per wafer	668	
Passivation front side	Polyimide	
Pad metal	AlCu (5µm)	
Backside metal	Al/Ti/Ni/Ag (2kÅ/2kÅ/3kÅ/4kÅ)	

Maximum Ratings

Parameter	**Symbol**	**Value**	**Unit**
Collector-Emitter voltage	V_{CE}	1050	V
DC collector current	I_C	200	A
Operating junction temperature	T_{vj}	-40 … +175 [a)]	°C
Gate emitter voltage	V_{GE}	±20	V

[a)] Tvj >150°C is allowed for operation at temporary overload conditions.

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Edited by Semi-Future Technologies. Edition 0.1
Publication: 2024-06-04

Preliminary

Static Characteristics (tested on wafer), T_{vj}=25°C

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Collector-Emitter breakdown voltage	$V_{(BR)CES}$	V_{GE}=0V, I_C=1mA	1050			V
Collector-Emitter saturation voltage	V_{CEsat}	V_{GE}=15V, I_C=200A		1.70	2.10	
Gate-Emitter threshold voltage	$V_{GE(th)}$	I_C=3.25mA, V_{GE}= V_{CE}	4.20	4.80	5.40	
Zero gate voltage collector current	I_{CES}	V_{CE}=1050V, V_{GE}= 0V			10	uA
Gate-Emitter leakage current	I_{GES}	V_{CE}=0V, V_{GE}= 20V			100	nA
Integrated gate resistor	r_G [a)]			1.50		Ω
Input capacitance	C_{ies} [a)]	V_{CE}=25V, V_{GE}=0V, f=100kHz		14.43		nF
Reverse transfer capacitance	C_{res} [a)]			0.05		

[a)] tested on device

Further Electrical Characteristic

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

Application example	S3L400R10GA7U

Chip Drawing

Unit：μm